IN THE ABSTRACT:

Please replace the abstract beginning on page 39, line 2 with the following:

A semiconductor device comprises a memory cell array and a word-line select circuit. The memory cell array includes a plurality of memory cells arranged in rows and columns, the memory cell array having a plurality of blocks in each one of which the memory cells are arranged. The word-line select circuit includes transfer transistors arranged in row and column directions, and configured to select at least one row of memory cells from the plurality of memory cells in a block. The word-line select circuit includes first transistors to which OV is to be applied, second transistors to which an intermediate level voltage is to be applied, the intermediate voltage being a voltage applied to a non-selected word line in a block selected in a writing operation, third transistors to which a write voltage is to be applied, the third transistors being separated from the first transistors.

~~A semiconductor memory device comprises a memory cell array, a block select circuit, a plurality of word line driving signal lines, and a plurality of transfer transistors. The memory cell array includes a plurality of blocks, each of the blocks including memory cells arranged in rows and columns. The block select circuit selects one of the blocks of the memory cell array. The word line driving signal lines receive voltages to be applied to a plurality of word lines in each block. The transfer transistors are connected between the word line driving signal lines and the word lines of the memory cell array, and are controlled by outputs from the block select circuit. Any two of the transfer transistors, which correspond to each pair of adjacent ones of the word lines, are separate from each other lengthwise and widthwise, and one or more transfer transistors corresponding to another word line or other word lines are interposed therebetween.~~